Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of distributing a clock signal over a transmission line, the method comprising:

providing a return line geometrically matched to the transmission line;

generating an output clock signal onto a transmission line;

detecting a returned clock signal on the return line;

detecting a first phase difference between a reference clock signal and the output clock signal;

detecting a second phase difference between the reference clock signal and the returned clock signal;

controlling the phase of the output clock signal based on an average of the first and second phase differences.

2. (currently amended) ~~A method, as set forth in claim 1, further comprising~~ A method of distributing a clock signal, the method comprising:

generating an output clock signal onto a transmission line;

detecting a ~~obtaining the~~ returned clock signal by sensing a reflection of the output clock signal on the transmission line;

detecting a first phase difference between a reference clock signal and the output clock signal;

detecting a second phase difference between the reference clock signal and the returned clock signal;

controlling the phase of the output clock signal based on an average of the first and second phase differences.

3. (canceled)

4. (previously presented) A method, as set forth in claim 2, wherein the reflected signal is sensed by comparing the output clock signal with a composite signal from the transmission line, the composite signal including the output clock signal and a reflection of the output clock signal from the destination.

5. (previously presented) A method, as set forth in claim 1, wherein the step of controlling the phase of the output clock signal comprises driving a voltage controlled oscillator using the average of the first and second phase differences.

6. (previously presented) A method, as set forth in claim 5, further comprising buffering the output of the voltage controlled oscillator.

7. (currently amended) ~~A method, as set forth in claim 5, further comprising~~ A method of distributing a clock signal, the method comprising:

generating an output clock signal onto a transmission line;

detecting a returned clock signal;

detecting a first phase difference between a reference clock signal and the output clock signal;

detecting a second phase difference between the reference clock signal and the returned clock signal;

controlling the phase of the output clock signal based on an average of the first and second phase differences by driving a voltage controlled oscillator using the average of the first and second phase differences; and

buffering the output of the voltage controlled oscillator and providing a build out impedance to match the transmission line impedance.

8. (canceled)

9. (currently amended) ~~The~~ A clock distribution circuit~~, as set forth in claim 8, further~~ comprising:

a first phase detector that outputs a phase lead of an output clock signal;

a second phase detector that outputs a phase lag of a returned clock signal;

circuitry that propagates the output clock signal onto a transmission line based on the average the output of the first phase detector and the second phase detector; and

circuitry to ~~detected~~ detect the returned clock signal as a reflected clock signal on the transmission line.

10. (currently amended) ~~The~~ A clock distribution circuit~~, as set forth in claim 8, further~~ comprising:

a first phase detector that outputs a phase lead of an output clock signal;

a second phase detector that outputs a phase lag of a returned clock signal;

circuitry that propagates the output clock signal onto a transmission line based on the average the output of the first phase detector and the second phase detector; and

a signal return line separate from the transmission line, wherein the returned clock signal is sensed from the signal return line.

11. (previously presented) The clock distribution circuit, as set forth in claim 10, wherein the signal return line is matched to the transmission line.

Amendments to the Drawings:

No amendments to the Drawings are requested herein.